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OWENS, DOUGLAS W	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 08/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/515,760	Applicant(s) MARR ET AL.	
	Examin r Douglas W Owens	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover she t with th correspond nce addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _16 May 2003_ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-52_ is/are pending in the application.

4a) Of the above claim(s) _19-26 and 47-52_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-18 and 27-46_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _12_ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6 and 43-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 5,811,869 to Seyyedy et al.

Regarding claim 1, Seyyedy et al. teaches an antifuse comprising:

a well of first conductivity type (12);

a first conductive terminal (22); and

an insulator (20) between the well and the conductive terminal.

Seyyedy et al. further teaches that the antifuse is formed as a capacitor using standard transistor fabrication techniques (Col. 3, lines 1-7). Seyyedy et al. does not teach a first conductive terminal of the second conductivity type. It would have been obvious to select either first or a second conductivity type for the first conductive terminal depending on the desired work function of the capacitor plate. Additionally, *since Seyyedy et al. is silent with respect to the conductivity type of the first conductive terminal*, one having ordinary skill in the art would have been required to select a conductivity type of either N or P, since they are the only two available and it has not been shown to be a critical feature of the invention.

Regarding claim 2, Seyyedy et al. teaches an antifuse, further comprising an Ohmic contact (16).

Regarding claim 3, Seyyedy et al. teaches an antifuse, wherein:

the substrate comprises p-type silicon;

the well is n-type;

the Ohmic contact is an n+ diffusion layer; and

the insulator layer is oxide.

Seyyedy et al. does not teach an antifuse, wherein the conductive terminal is a layer of p-type polysilicon. It would have been obvious to one of ordinary skill in the art to select p-type polysilicon for reasons discussed above.

Regarding claim 4, Seyyedy et al. teaches an antifuse, wherein:

the substrate is n-type;

the well is p-type;

the Ohmic contact is p+; and

the insulator is oxide.

Seyyedy et al. does not teach an antifuse wherein the well is p+ type and the conductive terminal is n-type. It would have been obvious to select an n-type or p-type terminal for reasons discussed above.

Regarding claim 5, Seyyedy et al. teaches an integrated circuit (Fig. 4) comprising:

a first circuit;

a second circuit; and

an antifuse (10) between the first and second circuit comprising:

a well of first conductivity type (12);

a first conductive terminal (22); and

an insulator (20) between the well and the conductive terminal.

Seyyedy et al. does not teach a first conductive terminal of the second conductivity type. It would have been obvious to select the second conductivity type for the first conductive terminal for reasons discussed above.

Regarding claim 6, Seyyedy et al. teaches an integrated circuit further comprising an Ohmic contact as a second conductive terminal.

Regarding claim 43, Seyyedy et al. teaches a method of forming an antifuse comprising:

forming a well of first conductivity type (12);

forming a first conductive terminal (22); and

forming an insulator (20) between the well and the conductive terminal.

Seyyedy et al. does not teach forming a first conductive terminal of the second conductivity type. It would have been obvious to select a second conductivity type for the first conductive terminal for reasons discussed above.

Regarding claim 44, Seyyedy et al. teaches method of forming an antifuse, further comprising forming an Ohmic contact (16) as a second conductive terminal.

Regarding claim 45, Seyyedy et al. teaches a method wherein forming the well comprises forming an n-type well in a p-type silicon substrate and further comprising:

forming an n+ drain region (18);

forming an n+ source region (16);

forming an oxide (20) between the source and drain diffusion regions; and

forming a conductive terminal (22) over the oxide.

Seyyedy et al. does not teach an antifuse, wherein the conductive terminal is a layer formed of p-type polysilicon. It would have been obvious to one of ordinary skill in the art to select p-type polysilicon for reasons discussed above.

Regarding claim 46, Seyyedy et al. teaches a method wherein forming the well comprises forming a p-type well in a n-type silicon substrate and further comprising (Fig. 2):

forming an p+ drain region;

forming an p+ source region;

forming an oxide (20) between the source and drain diffusion regions; and

forming a conductive terminal (22) over the oxide.

Seyyedy et al. does not teach a method wherein a p+-type well is formed and an n-type conductive terminal is formed. It would have been obvious to select an n-type or p-type terminal for reasons discussed above.

3. Claims 10-18 and 27-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seyyedy et al. in view of US patent No. 5,742,555 to Marr et al. Regarding claims 10 and 15, Seyyedy et al. teaches an integrated circuit comprising a plurality of antifuses, each antifuse comprising:

a well of first conductivity type (13);

a first conductive terminal (22); and

an insulator (20) between the well and the conductive terminal.

Seyyedy et al. does not teach a programming logic circuit and an external pin.

Marr et al. teaches an integrated circuit (Fig. 3) comprising:

a programming logic circuit; and

an external pin. It would have been obvious to employ the antifuse taught by Seyyedy in such a configuration since it is a commonly known circuit layout and it is desirable for the antifuse to have functionality. Additionally, this is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963))

Neither Seyyedy et al. nor Marr et al. teach a first conductive terminal of the second conductivity type. It would have been obvious to select a second conductivity type for the first conductive terminal for reasons discussed above.

Regarding claims 11 and 16, Seyyedy et al. does not teach an integrated circuit, further comprising an Ohmic contact in the well coupled to the external pin. Marr et al. teaches an integrated circuit, further comprising an Ohmic contact in the well coupled to the external pin. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Marr et al. into the device taught by Seyyedy et al. for reasons discussed above.

Regarding claims 12 and 17, Seyyedy et al. teaches an integrated circuit, wherein:

the substrate comprises p-type silicon;

the well is n-type;

the Ohmic contact is an n+ diffusion layer; and

the insulator layer is oxide.

Neither Seyyedy et al. nor Marr et al. teach an antifuse, wherein the conductive terminal is a layer of p-type polysilicon. It would have been obvious to one of ordinary skill in the art to select p-type polysilicon for reasons discussed above.

Regarding claims 13 and 18, Seyyedy et al. teaches an integrated circuit, wherein:

the substrate is n-type;

the well is p-type;

the Ohmic contact is p+; and

the insulator is oxide.

Neither Seyyedy et al. nor Marr et al. teach an antifuse wherein the well is p-type and the conductive terminal is n-type. It would have been obvious to select an n-type or p-type terminal depending on the desired work function of the capacitor plate. Additionally, one having ordinary skill would have been required to select one of an n-type or a p-type since they are the only two options.

Regarding claim 14, Seyyedy does not teach an integrated circuit, wherein the integrated circuit comprises a memory device, an array of memory cells, an address decoder, a plurality of I/O paths, and an I/O control circuit. Marr et al. teaches an integrated circuit, wherein the integrated circuit comprises a memory device, an array of memory cells, an address decoder, a plurality of I/O paths, and an I/O control circuit

(Fig. 5, Col. 4, lines 31-45). It would have been obvious to employ the antifuse taught by Seyyedy in such a configuration since it is a commonly known circuit layout. Additionally, This is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963))

Regarding claim 27, Seyyedy et al. does not teach a method comprising:

coupling a first programming voltage to a well of a first conductivity type; and

coupling a second programming voltage to a conductive terminal to create a conductive path through the insulator between the conductive terminal and the well to program the antifuse.

Marr et al. teaches a method comprising:

coupling a first programming voltage to a well of a first conductivity type; and

coupling a second programming voltage to a conductive terminal to create a conductive path through the insulator between the conductive terminal and the well to program the antifuse. It would have been obvious to one of ordinary skill in the art to use the programming method taught by Marr et al. since the structure of the device is identical to the device taught by Seyyedy et al.

Neither Seyyedy et al. nor Marr et al. teach a conductive terminal of the second conductivity type. It would have been obvious to select a second conductivity type for the conductive terminal depending on the desired work function of the capacitor plate, as well as for reasons discussed above.

Regarding claims 28, 32 and 40, Seyyedy et al. does not teach a method, wherein coupling a first programming voltage comprises coupling a first programming voltage to an Ohmic contact in the well of the first conductivity type. Marr et al. teaches a method, wherein coupling a first programming voltage comprises coupling a first programming voltage to an Ohmic contact in the well of the first conductivity type. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Regarding claims 29 and 41, Seyyedy et al. does not teach a method wherein:

coupling a first programming voltage comprises coupling a very high voltage to an n+ region; and

coupling a second programming voltage comprises coupling a ground voltage to the conductive terminal (Col. 3, lines 63 and 64), wherein the antifuse is programming by placing a potential across the thin oxide layer that is sufficient to rupture the oxide and short the well and conductive terminal together.

Marr et al. teaches a method, wherein:

coupling a first programming voltage comprises coupling a very high voltage to an n+ region; and

coupling a second programming voltage comprises coupling a ground voltage to the conductive terminal (Col. 3, lines 63 and 64), wherein the antifuse is programming by placing a potential across the thin oxide layer that is sufficient to rupture the oxide and short the well and conductive terminal together. It would have been obvious to one

of ordinary skill in the art to incorporate the teaching of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Neither Seyyedy et al. nor Marr et al. teach an antifuse, wherein the conductive terminal is a layer of p-type polysilicon. It would have been obvious to one of ordinary skill in the art to select p-type polysilicon for reasons discussed above.

Regarding claims 30 and 42, Seyyedy et al. does not teach a method wherein a very negative potential is coupled to a p+ diffusion region and a supply voltage is coupled to the polysilicon layer. Marr et al. teaches a method, wherein any combination of programming voltages can be utilized to provide the breakdown potential across the oxide layer. Marr et al. does not explicitly teach a method wherein a very negative potential is coupled to a p+ diffusion region and a supply voltage is coupled to the polysilicon layer. The combination of a negative potential to the p+ region and a supply voltage being coupled to the polysilicon layer is one of many combinations that would have provided a breakdown potential across the oxide layer. It would have been obvious to select such a combination since it is a known method of forming a large potential difference. It would have further been obvious to incorporate the teaching of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Neither Seyyedy et al. nor Marr et al. teach an antifuse wherein the well is p+-type and the conductive terminal is n-type. It would have been obvious design to select an n-type or p-type terminal depending on the desired work function of the capacitor plate, as well as for reasons discussed above.

Regarding claim 31, Seyyedy et al. does not teach a method comprising:

selecting an antifuse coupled between two circuits;

coupling a first programming voltage to a well of a first conductivity type; and

coupling a second programming voltage to a conductive terminal to create a conductive path through the insulator between the conductive terminal and the well to program the antifuse.

Marr et al. teaches a method of operating an integrated circuit comprising:

selecting an antifuse coupled between two circuits;

coupling a first programming voltage to a well of a first conductivity type; and

coupling a second programming voltage to a conductive terminal to create a conductive path through the insulator between the conductive terminal and the well to program the antifuse. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Neither Seyyedy et al. nor Marr et al. teach a conductive terminal of the second conductivity type. It would have been obvious to select a second conductivity type for the conductive terminal depending on the desired work function of the capacitor plate, as well as for reasons discussed above.

Regarding claims 33 and 37, Seyyedy et al. does not teach a method, wherein:

the antifuse is selected from a plurality of antifuses coupled between a programming logic circuit and an external pin coupled to a bias circuit;

coupling a first programming voltage comprises coupling a very high voltage to the external pin that is coupled to an n+ region; and

coupling a second programming voltage comprises coupling a ground voltage from the programming logic circuit to the conductive terminal (Col. 3, lines 63 and 64), wherein the antifuse is programming by placing a potential across the thin oxide layer that is sufficient to rupture the oxide and short the well and conductive terminal together.

Marr et al. teaches a method wherein:

the antifuse is selected from a plurality of antifuses coupled between a programming logic circuit and an external pin coupled to a bias circuit;

coupling a first programming voltage comprises coupling a very high voltage to the external pin that is coupled to an n+ region; and

coupling a second programming voltage comprises coupling a ground voltage from the programming logic circuit to the conductive terminal (Col. 3, lines 63 and 64), wherein the antifuse is programmed by placing a potential across the thin oxide layer that is sufficient to rupture the oxide and short the well and conductive terminal together. It would have been obvious to one of ordinary skill in the art to incorporate the method of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Neither Seyyedy et al. nor Marr et al. teach an antifuse, wherein the conductive terminal is a layer of p-type polysilicon. It would have been obvious to one of ordinary skill in the art to select p-type polysilicon for reasons discussed above.

Regarding claims 34 and 38, Seyyedy et al. does not teach a method wherein:

the antifuse is selected from a plurality of antifuses coupled between a programming logic circuit and an external pin coupled to a bias circuit; and

wherein any combination of can be utilized to provide the breakdown potential across the oxide layer.

Marr et al. teaches a method wherein:

the antifuse is selected from a plurality of antifuses coupled between a programming logic circuit and an external pin coupled to a bias circuit; and

wherein any combination of can be utilized to provide the breakdown potential across the oxide layer.

Marr et al. does not explicitly teach a method wherein a very negative potential is coupled to a p+ diffusion region and a supply voltage is coupled to the polysilicon layer. The combination of a negative potential to the p+ region and a supply voltage being coupled to the polysilicon layer is one of many combinations that would have provided a breakdown potential across the oxide layer. It would have been obvious to select such a combination since it is one of many known combinations that would have resulted in creating a breakdown potential across the oxide. It would have further been obvious to incorporate the teaching of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Neither Seyyedy et al. nor Marr et al. teach an antifuse wherein the well is p+-type and the conductive terminal is n-type. It would have been obvious to select an n-type or p-type terminal for reasons discussed above.

Regarding claim 35, Seyyedy et al. does not teach a method of operating an integrated circuit comprising:

selecting an antifuse coupled between a circuit and an external pin;

coupling a first programming voltage to the external pin that is coupled to the well of a first conductivity type; and

coupling a second programming voltage from the circuit to a conductive terminal to create a conductive path through the insulator between the conductive terminal and the well to program the antifuse.

Marr et al. teaches a method of operating an integrated circuit comprising:

selecting an antifuse coupled between a circuit and an external pin;

coupling a first programming voltage to the external pin that is coupled to the well of a first conductivity type; and

coupling a second programming voltage from the circuit to a conductive terminal to create a conductive path through the insulator between the conductive terminal and the well to program the antifuse. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Regarding claim 36, Seyyedy et al. does not teach a method, wherein coupling a first programming voltage comprises coupling a first programming voltage the external pin coupled to an Ohmic contact in the well of the first conductivity type.

Marr et al. teaches a method, wherein coupling a first programming voltage comprises coupling a first programming voltage the external pin coupled to an Ohmic contact in the well of the first conductivity type. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Regarding claim 39, Seyyedy et al. does not teach a method comprising:

selecting circuits to be coupled together;

programming an antifuse using a method comprising:

coupling a first programming voltage to a well of a first conductivity type; and

coupling a second programming voltage to a conductive terminal to create a conductive path through the insulator between the conductive terminal and the well to program the antifuse.

Marr et al. teaches a method comprising:

selecting circuits to be coupled together;

programming an antifuse using a method comprising:

coupling a first programming voltage to a well of a first conductivity type; and

coupling a second programming voltage to a conductive terminal to create a conductive path through the insulator between the conductive terminal and the well to program the antifuse. It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Marr et al. into the teaching of Seyyedy et al. for reasons discussed above.

Neither Seyyedy et al. nor Marr et al. teach a conductive terminal of the second conductivity type. It would have been obvious to select a second conductivity type for the conductive terminal for reasons discussed above.

4. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seyyedy as applied to claims 5 and 6 above, and further in view of US patent No. 5,742,555 to Marr et al.

Regarding claim 7, Seyyedy et al. teaches an integrated circuit, wherein:

the substrate comprises p-type silicon;

the well is n-type;

the Ohmic contact is an n+ diffusion layer; and

the insulator layer is oxide.

Seyyedy et al. does not teach a programming logic circuit and an external pin. Marr et al. teaches an integrated circuit (Fig. 3) comprising:

a programming logic circuit; and

an external pin. It would have been a matter of obvious design choice to employ the antifuse taught by Seyyedy in such a configuration since it is desirable to add functionality to the antifuse device and this is a commonly known circuit layout. Additionally, This is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963))

Seyyedy et al. does not teach an antifuse, wherein the conductive terminal is a layer of p-type polysilicon. It would have been obvious to one of ordinary skill in the art to select p-type polysilicon for reasons discussed above.

Regarding claim 8, Seyyedy et al. teaches an integrated circuit, wherein:

the substrate is n-type;

the well is p-type;

the Ohmic contact is p+; and

the insulator is oxide.

Seyyedy et al. does not teach a programming logic circuit and an external pin. Marr et al. teaches an integrated circuit (Fig. 3) comprising:

a programming logic circuit; and

an external pin. It would have been a matter of obvious design choice to employ the antifuse taught by Seyyedy in such a configuration since it is a commonly known circuit layout. Additionally, This is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963))

Seyyedy et al. does not teach an antifuse wherein the well is p-type and the conductive terminal is n-type. It would have been a matter of obvious design choice to select an n-type or p-type terminal depending on the desired work function of the capacitor plate.

Regarding claim 9, Seyyedy does not teach an integrated circuit, wherein the integrated circuit comprises a memory device, an array of memory cells, an address decoder, a plurality of I/O paths, and an I/O control circuit. Marr et al. teaches an integrated circuit, wherein the integrated circuit comprises a memory device, an array of memory cells, an address decoder, a plurality of I/O paths, and an I/O control circuit (Fig. 5, Col. 4, lines 31-45). It would have been a matter of obvious design choice to employ the antifuse taught by Seyyedy in such a configuration since it is a commonly known circuit layout. Additionally, This is considered a suggested use limitation and is not given any patentable weight. (See In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967);In re Otto, 312 F.2d 937, 938, 136 USPQ 458, 459 (CCPA 1963)).

Response to Arguments

4. Applicant's arguments filed May 16, 2003 have been fully considered but they are not persuasive.

The applicant argues that there is no motivation cited in the prior art that supports motivation for modifying Seyyedy. To establish a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. It is well-known in the art that polysilicon may be doped one of two types, n-type or p-type. There is no other dopant type to choose from. Seyyedy is silent with regard to the type of dopant used for the conductive terminal. One having ordinary skill would have been required to select one of the two known types of dopants. Additionally, there is no showing that the conductivity type of the conductive terminal is a critical feature of the invention.

It is also known that the type of dopant may be selected according to the desired work function. There is a discussion of the work function on pages 428 – 434 by Donald Neamen, Semiconductor Physics & Devices, particularly on page 431. A copy has been included for the Applicant's convenience.

The Applicant argues that there is no motivation set forth for modifying the device taught by Seyyedy et al. with respect to the dopant type of the gate. As discussed above, Seyyedy et al. does not disclose the dopant type of the gate. There are only two dopant types available. Neamen discusses the two types of available dopants in pages 96 – 98 of Semiconductor Physics & Devices, which has been included for the

Applicant's convenience. Since Seyyedy et al. is silent with respect to the dopant type used, one having ordinary skill in the art would have been highly motivated to select one of the two. The only other option would have been not to complete fabrication of the device. Indeed, it is not known why one having ordinary skill would choose not to select a dopant type.

The Applicant argues that there is no motivation provided for combining Marr et al. with Seyyedy et al. As stated above, it is desired to give the device functionality. The purpose of the antifuse is to provide shorts and opens between circuit devices. Marrr et al. teaches a common use of the antifuse in the function it is designed to perform. There are many patents showing that it is common to use an antifuse in a circuit configuration including a programming logic circuit and external pin, as evidenced in the following US patents:

5,841,789 to McClure (See Col. 6, lines 21 – 36 for example, and the figures)
6,247,088 to Seo et al. (Figures, abstract and Col. 17, lines 31 – 44)
6,242,941 to Vest et al. (Figures, Col. 1, line 63 – Col. 2, line 13; Col. 6, lines 40 – 51)
5,917,229 to Nathan et al. (Figures, abstract; Col. 1, lines 32 – 43)
5,751,162 to Mehendale et al. (See Figures)
Also see patents to Jacobson et al., Teggatz et al., Yip et al., Nagaraj, McClure and Galbraith.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Douglas W Owens whose telephone number is 703-308-6167. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for

the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DWO
July 17, 2003

Steven Loke
Primary Examiner
Steven Loke